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Power MOSFET Switching Waveforms: A New Insight

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The examination of power MOSFET voltage and current waveforms during switching transitions reveals that the device characterization now practiced by industry is inadequate. In this Note, device waveforms are explained by considering the interaction of a vertical JFET driven in cascode from a lateral MOSFET in combination with the interelectrode capacitances. Particular attention is given to the drain-voltage waveform and its dual-slope nature. The three terminal capacitances now published by the industry are shown to be valid only for zero drain current. For cases where the gate drive is a voltage step generator with internal fixed resistance, the drain voltage characteristics are inferred from the gate current drive behavior and compared to observed waveforms. The nature of the "asymmetric switching times" is explained.

A waveform family is proposed as a more descriptive and accurate method of characterization. This new format is a plot of drain voltage and gate voltage versus normalized time. A family of curves is presented for a constant load resistance with V_{DS} varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

Device Models

The keystone of an understanding of power MOSFET switching performance is the realization that the active device is bimodal and must be described using a model that accounts for the dual nature. Buried in today's power MOSFET devices is the equivalent of a depletion layer JFET that contributes significantly to switching speed. Figure 1 is a cross-sectional view of a typical power MOSFET, with MOSFET/JFET symbols superimposed on the structure.

Figure 2 is obtained by taking the lateral MOS and vertical JFET from this conception and adding all the possible node-to-node capacitances. Computed values of the six capacitances for a typical device structure suggest that device behavior may be adequately modeled using only three capacitors in the manner of Figure 3. This is the model to be employed for analysis and study.

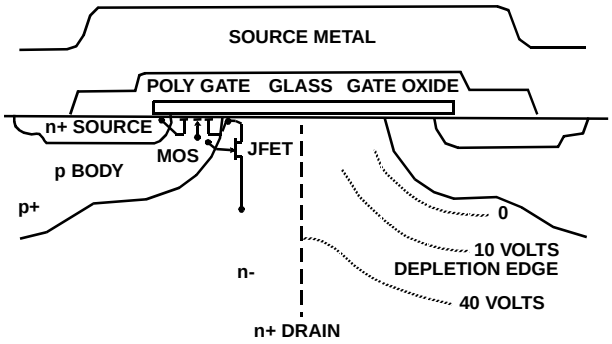


FIGURE 1. CROSS-SECTION VIEW OF MOSFET SHOWING EQUIVALENT MOS TRANSISTOR AND JFET

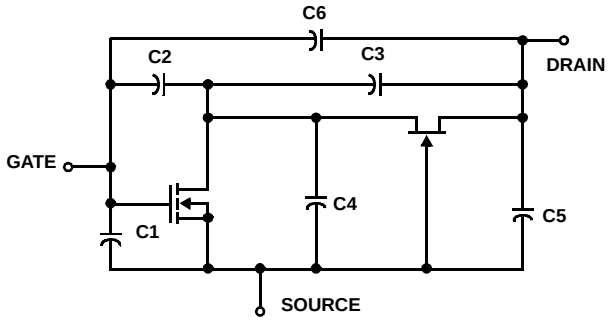


FIGURE 2. MOS TRANSISTOR WITH CASCODE-CONNECTED JFET AND ALL CAPACITORS

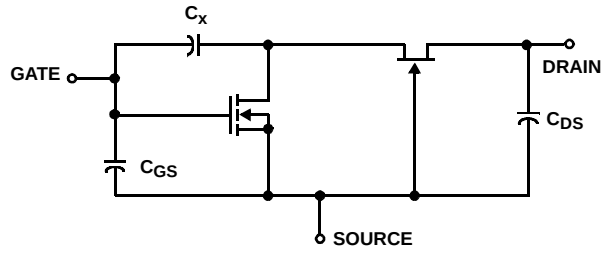


FIGURE 3. FIGURE 2 SIMPLIFIED

Gate Drive: Constant Voltage or Constant Current

Before moving on to the study of the equivalent circuit states of the model, a gate-drive forcing function which is easy to represent, relates to reality, and best illustrates device behavior must be chosen. The choice may be immediately narrowed to two:

(1) An instantaneous step voltage with internal resistance R, Figure 5.

(2) An instantaneous step current with infinite internal resistance, Figure 6.

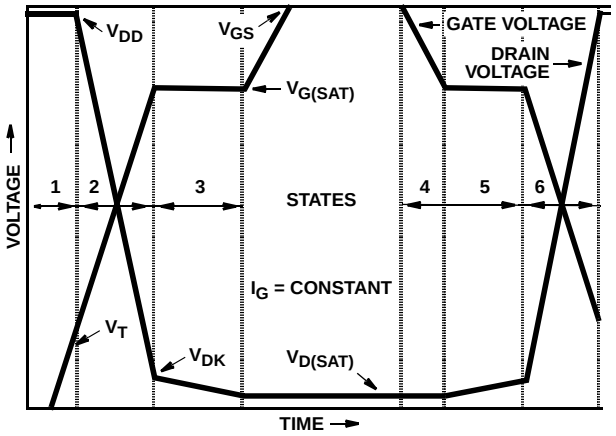


FIGURE 4. IDEALIZED POWER MOSFET WAVEFORMS

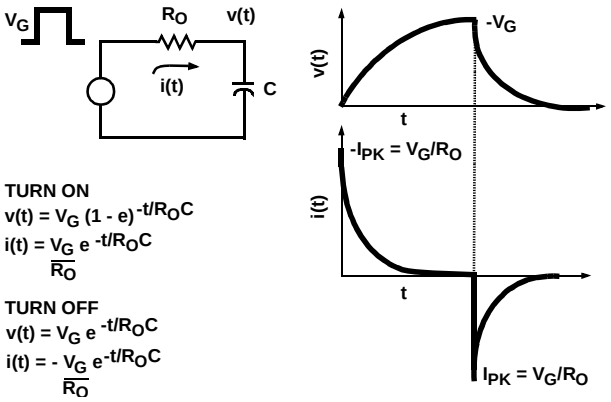


FIGURE 5. STEP-VOLTAGE FORCING FUNCTION

Power MOSFET devices are highly capacitive in nature; hence, simple capacitor responses to the forcing functions offer a good vehicle for comparison. The advantageous choice is immediately obvious: Figure 6. Voltage/time responses dominated by capacitance are straight lines (when constant current is used). The slope of these lines is proportional to current and inversely proportional to capacitance. Analytically, then, constant current is most convenient. It is quite another matter, however, to build a bidirectional current drive that is accurate across the many decades of both current and time required to establish experimental verification.

Six States

To completely characterize power MOSFET switching waveforms, the six states that a device assumes, Figure 6, must be addressed:

STATE	MOS	JFET
Turn-on 1	Off	Off
Turn-on 2	Active	Active
Turn-on 3	Active	Saturated†
Turn-off 4	Saturated	Saturated†
Turn-off 5	Active	Saturated
Turn-off 6	Active	Active

†The term saturated is taken to mean a constant low-voltage drain-source condition.

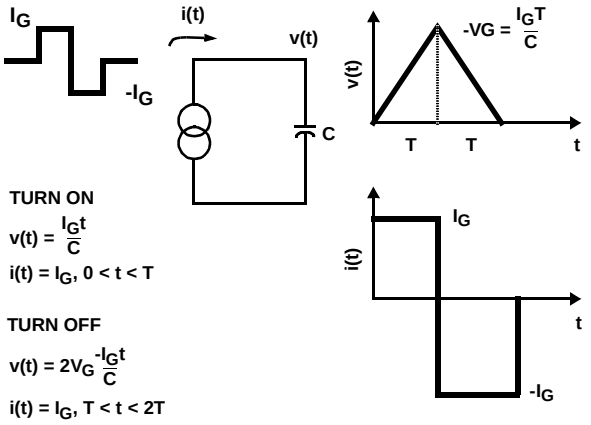
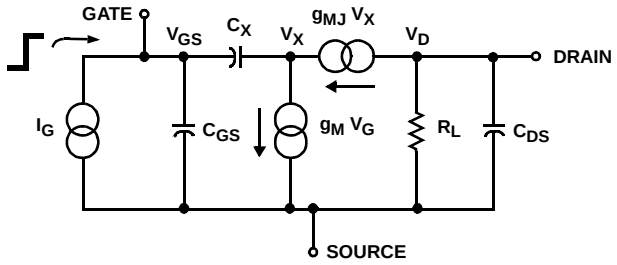


FIGURE 6. STEP CURRENT FORCING FUNCTION

Equivalent Circuit

The lumped-parameter model of Figure 3, with the cascode-connected JFET, can now be reduced to the linear equivalent circuit of Figure 7, and the six device states investigated from full off to full on.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_M	- MOSFET Transconductance
V_D	- Drain Voltage	g_{MJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_X	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE 7. POWER MOSFET EQUIVALENT CIRCUIT

State 1: MOS Off, JFET Off

In a power-MOSFET device, no drain current will flow until the device's gate threshold voltage, $V_{gs(TH)}$, is reached. During this time, the gate's current drive is only charging the gate source capacitance. More accurately, I_G is charging C_{ISS} ($C_{ISS} = C_{GS} + C_{GD}$, C_{DS} shorted), the capacitance designation published by the industry.

The current generators, $g_M V_G$ and $g_{MJ} V_X$ are open circuits for zero drain current, and R_L is presumed to be so low as to represent a short circuit (generally true for practical applications). This is academic however since C_{GS} is very much larger that C_X. The time to reach threshold, then, is simply:

$$T_1 = \frac{C_{ISS}\, V_{gs(TH)}}{I_G}$$

State 2: MOS ActIve, JFET ActIve

This state graphically illustrates the dramatic influence that the JFET has on the power MOSFET drain-voltage waveform. Instead of having to discharge C_x from V_{DD} to ground, the lateral MOSFET need only swing V_X to ground, a much smaller voltage thanks to the grounded gate JFET. Since the interaction of R_L with the device capacitances has a second-order effect on the drain voltage, the equivalent circuit of Figure 7 predicts a drain voltage change of:

$$dV_G/dt = g_M R_L I_G/[C_{GS} + C_X(1 + g_M/g_{MJ})]$$

In all but the smallest power-MOSFET devices, C_x is several thousand picofarads and g_M/g_{MJ} is of the order of 3:1. Power-MOSFET devices exhibit a high dV_D/dt switching rate because of the cascode-connected JFET, not because C_{RSS} ($C_{RSS} = C_{GD}$) is a small value, as zero-drain-current data sheet capacitance values might lead one to believe. If C_{RSS} were, in actuality, small, long drain voltage tails would not exist. The tail response is a direct result of JFET saturation. In order to delineate the transition from state 2 to state 3, a drain voltage at which the transition occurs must be defined. V_{DK} is the knee voltage at which linear extrapolations of drain-voltage slopes intersect. The time duration of state 2 is:

$$t_2(t_6) = (V_{DD} - V_{DK})[C_{GS} + C_X(1 + g_M/g_MJ)]/g_M R_L I_G$$

State 3: MOS Active, JFET Saturated

When the JFET saturates, the $g_{MJ}V_X$ current generator becomes a short circuit and the equivalent circuit predicts:

$$dV_D/dt = g_M R_L I_G/[C_{GS} + C_X(1 + g_M R_L)]$$

This is the Miller effect so often referred to in older texts that describe the behavior of grounded-cathode vacuum-tube amplifier circuits. Allowing for the fact that $1 + g_M R_L$ is approximately equal to $g_M R_L$ and $C_X(1 + g_M R_L)$ is very much larger than C_{GS}, the expression for drain-voltage tail time is:

$$t_3(t_5) = (V_{DK} - V_{D(SAT)})C_x/I_G$$

State 4: MOS Saturated, JFET Saturated (Turn-Off)

In this state, in addition to $g_{MJ}V_X$ being shorted, the $g_M V_G$ current generator is shorted, and I_G is occupied with charging C_X and C_{GS}, in parallel, from the peak value of V_G to $V_{G(SAT)}$. The time required for this is:

$$t_4 = (V_G - V_{G(SAT)})(C_{GS} + C_x)/I_G$$

Since a value for C_{GS} may be measured independently of switching time, the method described is the simplest way of determining C_X.

On turn-off, the state time equations are equally applicable, but in reverse order (states 5 and 6); see the idealized waveform of Figure 4.

Experimental Verification

The four switching states just analyzed indicate that for a given device, all four switching state times are inversely proportional to the magnitude of the gate drive current. Figure 8 illustrates the switching performance of a typical power MOSFET across three decades of gate drive current and time. In each case the data slope is almost a perfect -1.

A New Device Characterization

Figure 8 could not be a reasonable device data sheet presentation because it does not give the designer any information on a typical value for C_X, nor does it convey how V_{DK}, g_M, g_M/g_{MJ}, and V_G(sat) vary with drain current. What would be of enormous value to the designer is a plot of $V_D(t)$, $V_G(t)$ for selected values of V_{DD} and I_D within device ratings.

A reasonable characterization would be as follows:

1. The x axis would be normalized in terms of gate current drive.
2. The y axis would be normalized in terms of percent maximum rated BV_{DSS} (0 to 100%).
3. $R_L = BV_{DSS}/I_{D(max)}$ would define the drain load resistance.
4. Four plots of $V_D(t)$, $V_G(t)$ at 100%, 75%, 50%, and 25% $BV_{DSS(max)}$ would be shown.

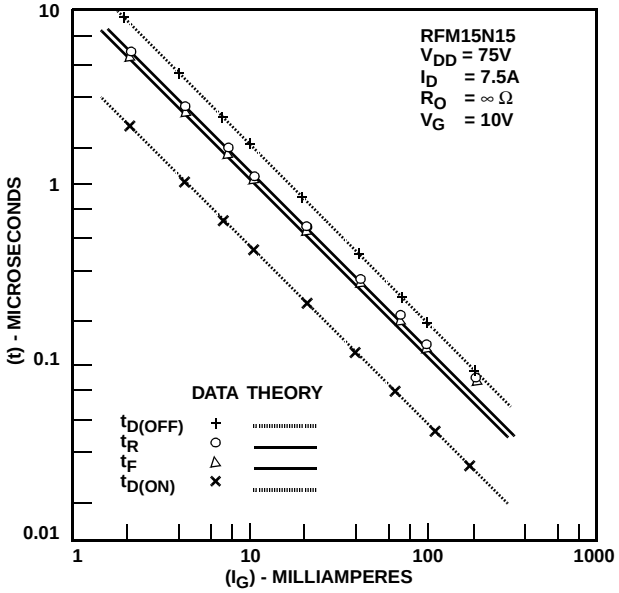


FIGURE 8. CONSTANT GATE CURRENT SWITCHING TIME

Figure 9 is such a plot for the RFM15N15 power MOSFET. With such a plot, a designer can estimate device switching performance under any resistive gate/drain conditions.

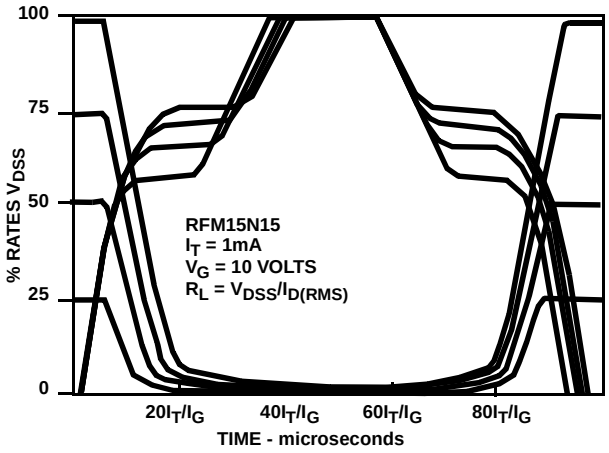


FIGURE 9. NORMALIZED RFM15N15 SWITCHING WAVEFORMS FOR CANSTANT GATE-CURRENT DRIVE.

Step-Voltage Gate Drive

The majority of power MOSFET applications employ a step gate-voltage input with a finite source resistance R_O. Often R_O for turn-on is not the same as R_O for turn-off. How can switching times for these situations be estimated using the switching characterization curves just described? The analysis for resistive step voltage inputs, which is complex because the gate current is no longer constrained to be constant, but is a function of device gate-voltage response, is covered in Appendix A. (A second, shorter appendix, B, has been added to illustrate the estimation of R_O for some practical gate drive circuits.) Table 1 summarizes the common switching equations, and indicates the appropriate 1_G to be used in each state for relating step voltage drives to the characterization curves.

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_O$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table 1, the observed differences between Figures 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current V_G/R_O equalling the constant I_G, $t_{D(on)}$, t_R, $t_{D(off)}$, and t_F will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t_R, t_F switching symmetry is disrupted by the use of a step voltage with source resistance R_O. For states 2 and 6 the time ratio is:

TABLE 1. COMMON SWITCHING EQUATIONS

	CONSTANT CURRENT	STATE 1: MOS OFF, JFET OFF	CONSTANT VOLTAGE
TURN ON	$t = \frac{C_{ISS} V_{GS(TH)}}{I_G}$		$t = R_O C_{ISS} \ln \frac{[1]}{[1 - V_{GS(TH)}/V_G]}$
	$I_G = I_T$	STATE 2: ACTIVE, ACTIVE	$I_G = (V_G - V_{GS(TH)})/R_O$
	$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_M/g_{MJ})]}{g_M R_L I_G}$		
	$I_G = I_T$	STATE 3: ACTIVE, SATURATED	$I_G = (V_G - V_{G(SAT)})/R_O$
	$t = \frac{(V_{DK} - V_{D(SAT)})C_X}{I_G}$		
TURN OFF	$I_G = I_T$	STATE 4: SATURATED, SATURATED	$I_G = -V_G/R_O$
	$t = \frac{(C_{GS} + C_X)(V_G - V_{G(SAT)})}{I_G}$		$t = R_O(C_{GS} + C_X) \ln (V_G/V_{G(SAT)})$
	$I_G = I_T$	STATE 5: ACTIVE, SATURATED	$I_G = (V_G - V_{G(SAT)})/R_O$
	$t = \frac{(V_{DK} - V_{D(SAT)})C_X}{I_G}$		
	$I_G = I_T$	STATE 6: ACTIVE, ACTIVE	$I_G = (V_G - V_{G(SAT)})/R_O$
	$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L I_G}$		

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_O$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table 1, the observed differences between Figures 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current V_G/R_O equalling the constant I_G, $t_D(on)$, t_R, $t_D(off)$, and t_F will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t_R, t_F switching symmetry is disrupted by the use of a step voltage with source resistance R_O. For states 2 and 6 the time ratio is:

$$\frac{t_{TURN\text{-}ON}}{t_{TURN\text{-}OFF}} = \frac{V_{G(SAT)}}{V_G - V_{GS(TH)}}$$

For states 3 and 5 the time ratio is:

$$\frac{t_{TURN\text{-}ON}}{t_{TURN\text{-}OFF}} = \frac{V_{G(SAT)}}{V_G - V_{G(SAT)}}$$

Utilization of available maximum gate drive voltage and current can be optimized for fastest power MOSFET switching speed through the use of constant-current gate drive at the expense of increased gate-drive circuit complexity.

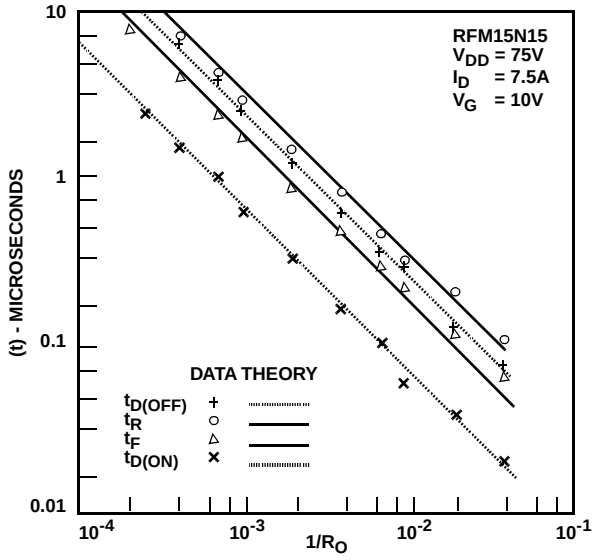


FIGURE 10. CONSTANT GATE VOLTAGE SWITCHING TIME

Using the Characterization Curve, Figure 9

To estimate the switching times for an RFM15N15 power MOSFET under the conditions V_G = 10V, V_{DD} = 75V, R_O = 100 ohms, and R_L = 10 ohms, precedes as follows:

State 1: MOS Off, JFET Off

This time can be estimated without recourse to the curves

$t = 100(1200 \times 10^{-12}) \ln [1/(1 - 4/10)]$

$t = 61$ ns

State 2 & 6: MOS Active, JFET Active

$I_G = (10 - 4)/100 = 60$mA

$$t = \frac{\text{(curve divisions)} \times I_T\ \mu s}{60} = \frac{9}{60} = 150\text{ns}$$

State 3: MOS Active, JFET Saturated

$I_G = (10 - 7)/100 = 30$mA

$$t = \frac{\text{(curve divisions)} \times I_T\ \mu s}{30} = \frac{14}{30} = 467\text{ns}$$

State 4: MOS Saturated, JFET Saturated

$C_{GS} + C_X$ = (gate voltage slope)(test current)

= $(1.5 \times 10^{-6}$s/5 volts)(10mA)

= 3000pF

$t = 100(3000 \times 10^{-12}) \ln [10/6.6]$

$t = 125$ns

State 5: MOS Active, JFET Saturated

$I_G = 6.6/100 = 66$mA

$$t = \frac{\text{(curve divisions)} \times I_T\ \mu s}{66} = \frac{8}{66} = 121\text{ns}$$

Figure 11 shows RFM15N15 waveforms using the conditions specified in the example.

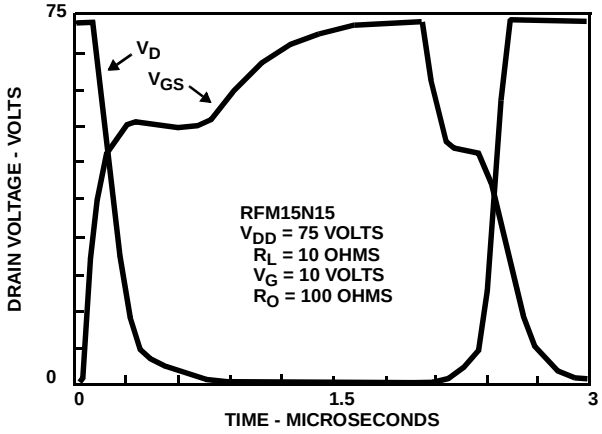


FIGURE 11. STEP GATE VOLTAGE INPUT TO AN RFM15N15

STATE	CALCULATED TIME	MEASURED TIME	RATIO
	(t_C, ns)	(t_M, ns)	(t_C/t_M)
1	61	60	1.02
2 + 3	617	670	0.92
4	125	137	0.91
5 + 6	271	375	0.72

For peak gate voltages other than 10 volts, and load resistances other than $BV_{DSS}/I_{D(MAX)}$, the equations of Table 1 may be used in conjunction with slope estimates from the characterization curves for C_X and $C_{GS} + C_X(1 + g_M/g_{MJ})$ at the appropriate drain-current level.

Characterization-Curve Limits

The switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of microamperes, device dissipation is the limiting factor. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. However, as Figure 12 graphically shows, the characterization is valid across five decades of gate current and switching time, allowing all but a very few switching applications to be described by the characterization curves of Figure 9.

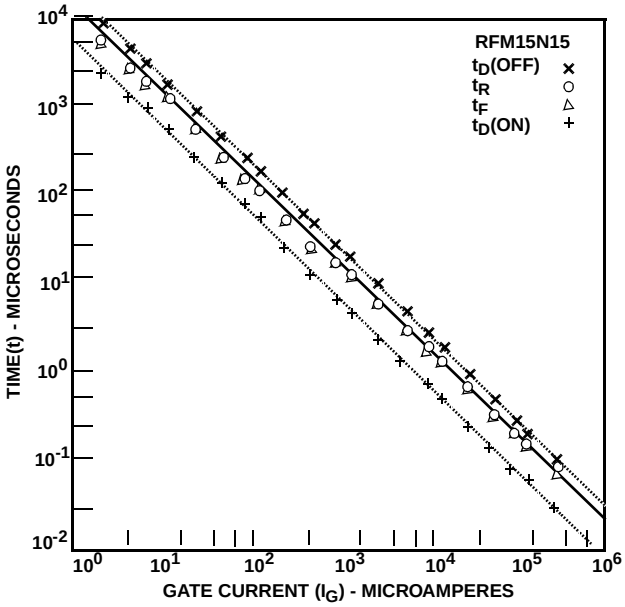


FIGURE 12. FIVE DECADES OF LINEAR RESPONSE

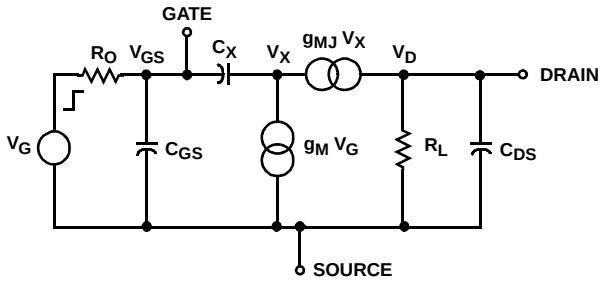
Conclusions

The viability of the proposed characterization curves using constant current has been demonstrated and the limits of application defined. The existence of a vertical JFET in a power MOSFET makes data-sheet capacitances of little use for estimating switching times. The classical method of defining switching time by 10% and 90% is a poor representation for power MOSFETs because of the dual-slope nature of the drain waveforms. Switching influences are masked because the 10% level is controlled by one mechanism and the 90% level by another. Device comparisons based on the classical switching definition can be very misleading.

Appendix A - Analysis for Resistive Step Voltage Inputs

Step Voltage Gate Drive

To obtain the necessary relationships, six device switching states must be examined using the same device equivalent circuit as was used for the constant-gate-current case, but with the forcing function replaced wIth a step voltage with internal resistance R_O, Figure A-1.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_M	- MOSFETTransconductance
V_D	- Drain Voltage	g_{MJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_X	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE A-1. POWER MOSFET EQUIVALENT CIRCUIT

State 1: Mos Off, JFET Off

As before, both current generators are open circuits, reducing the equivalent circuit to simply charging C_{ISS} through R_O.

$$t = R_O C_{ISS} \ln(1/(1 - V_{GS(TH)}/V_G))$$

State 2: Mos Active, JFET Active

Before proceeding, it is wise to examine an actual device response and make use of available simplifications. Figure A-2 shows $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage. For truly resistive switching, realize that these waveforms are only mirror images of their voltage counterparts $v_G(t)$ and $v_D(t)$. Using Figure A-2, applicable gate currents for each of the device states may be listed.

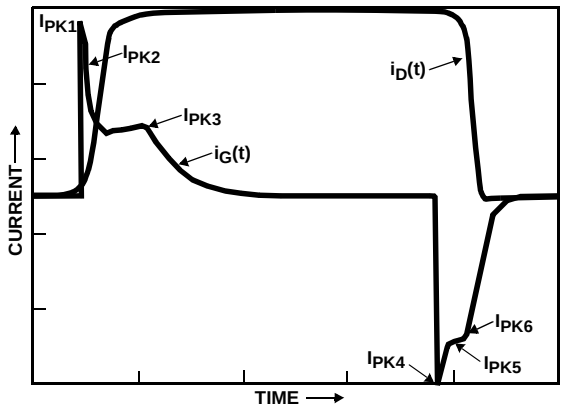


FIGURE A-2. $i_G(t)$ AND $i_D(t)$ FOR A TYPICAL POWER MOSFET DRIVEN BY A STEP GATE VOLTAGE

Turn-On

State 1: MOS Off, JFET Off

$I_{PK1} = V_G/R_O$

State 2: MOS Active, JFET Active

$I_{PK2} = (V_G - V_{GS(TH)})/R_O$

State 3: MOS Active, JFET Saturated

$I_{PK3} = (V_G - V_{G(SAT)})/R_O$

Turn-Off

State 4: MOS Saturated, JFET Saturated

$I_{PK4} = V_G/R_O$

State 5: MOS Active, JFET Saturated

$I_{PK5} = V_{G(SAT)}/R_O$

State 6: MOS Active, JFET Active

$I_{PK6} = V_{G(SAT)}/R_O$

The equivalent circuit of Figure A-1 predicts that:

$$dV_D/dt = (-g_M R_L(V_G - V_{GS(TH)})e^{-t/T1}) /T1$$

where $T1 = R_O C_{GS} + (1 + g_M/g_{MJ})R_O C_X$

Note that $g_M R_L(V_G - V_{GS(TH)})$ is usually an order of magnitude greater than V_{DD}, indicating that the drain voltage is discharging toward a very large negative value. The device operation, then, is on the early, almost linear, portion of the exponential, where $e^{-t/T1}$ approximates unity. The drain current of Figure A-2, and hence the drain voltage, does indeed exhibit a linear decrease with time.

Thus, for state 2:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L I_{PK2}}$$

where $I_{PK2} = (V_G - V_{GS(TH)})/R_O$

State 3: Mos Active, JFET Saturated

Because of the Miller effect, the gate voltage and, hence, the gate current, is almost constant during the tail time. The equivalent circuit then predicts:

$$\frac{dV_D}{dt} = \frac{g_M R_L I_G}{C_{GS} + (1 + g_M R_L)C_X} = \frac{I_G}{C_X}$$

$I_G = I_{PK3} = (V_G - V_{G(SAT)})/R_O$

and $t = \frac{(V_{DK} - V_{D[SAT]})C_X}{I_{PK3}}$

State 4: Mos Saturated, JFET Saturated (Turn-off)

Both equivalent-circuit generators are short circuits, and the gate drive is discharging C_X in parallel with C_{GS} through R_O.

$$t = R_O(C_{GS} + C_X)\ln[V_G/V_{G(SAT)}]$$

$$I_{PK4} = V_G/R_O$$

State 5: Mos Active, JFET Saturated

The JFET current generator $V_x g_{mJ}$, is operative.

$$t = \frac{[V_{DK} - V_{D[SAT]}]C_X}{I_{PK5}}$$

$I_{PK5} = V_{G(SAT)}/R_O$

State 6: Mos Active, JFET Active

The Miller effect is now reduced by the activation of $V_G g_{MJ}$, and the equivalent circuit predicts:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_M/g_{MJ})]}{g_M R_L I_{PAK6}}$$

$I_{PAK6} = V_{G(SAT)}/R_O$

Appendix B - Estimating R_O for Some Typical Gate-Drive Circuits

Case 1: Typical Pulse-Generator Drive, Figure B-1

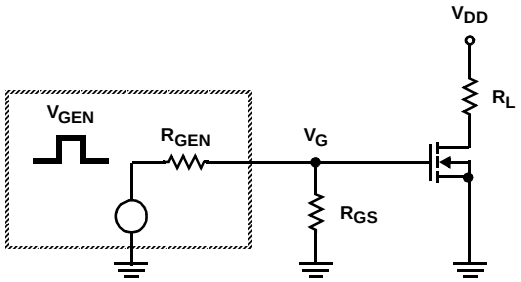


FIGURE B-1. TYPICAL PULSE-GENERATOR DRIVE CIRCUIT

Turn-On and Turn-Off

$$R_O = R_{GEN}R_{GS}/(R_{GEN} + R_{GS})$$

For the typical case where $R_{GEN} = 50\Omega$, and a coaxial-cable termination of 50 ohms, $R_O = 25\Omega$ and $V_G = V_{GEN}/2$.

Case 2: Voltage-Follower Gate Drive, Figure B-2

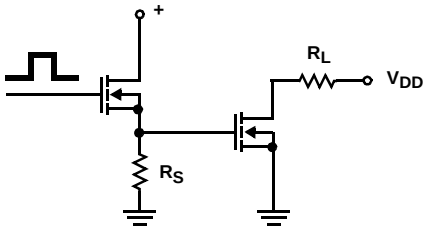


FIGURE B-2. VOLTAGE-FOLLOWER GATE-DRIVE CIRCUIT

Turn-On

R_O is approximately equal to $1/g_M$ for R_S very much greater than $1/g_M$.

gm = transconductance of driving MOSFET transistor.

Turn Off

$R_O = R_S$

Case 3 :Common-Source Gate Drive, Figure B-3

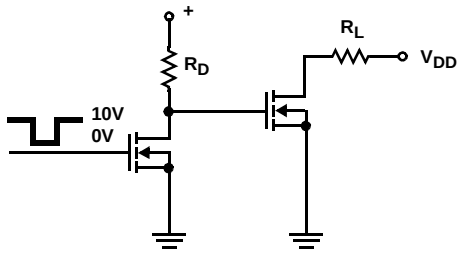


FIGURE B-3. COMMON-SOURCE GATE-DRIVE CIRCUIT

Turn-On

$R_O = R_D$

(drain-to-ground capacitance of driving device adds to C_{GS} of driven MOSFET.)

Turn Off

$R_O = r_{DS(ON)}$ of driving MOSFET when

R_D is very much greater than $R_{DS(ON)}$

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